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PETITION FEE
Under 37 CFR 1.17(f), (g) & (h)
TRANSMITTAL
(Fees are subject to annual revision)

Send completed form to: Commissioner for Patents
P.O. Box 1450, Alexandria, VA 22313-1450

Application Number	**10/767,074**
Filing Date	**January 30, 2004**
First Named Inventor	**Nobuyuki MINOWA**
Art Unit	
Examiner Name	
Attorney Docket Number	**1309.43464X00**

Enclosed is a petition filed under 37 CFR §1.102(d) that requires a processing fee (37 CFR 1.17(f), (g), or (h)). Payment of $ 130.00 is enclosed.

This form should be included with the above-mentioned petition and faxed or mailed to the Office using the appropriate Mail Stop (e.g., Mail Stop Petition), if applicable. For transmittal of processing fees under 37 CFR 1.17(i), see form PTO/SB/17i.

Payment of Fees (small entity amounts are NOT available for the petition (fees)

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☐ petition fee under 37 CFR 1.17(f), (g) or (h) ☒ any deficiency of fees and credit of any overpayments
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Petition Fees under 37 CFR 1.17(f): Fee $400 Fee Code 1462
For petitions filed under:
§ 1.53(e) - to accord a filing date.
§ 1.57(a) - to according a filing date.
§ 1.182 – for decision on a question not specifically provided for.
§ 1.183 – to suspend the rules.
§ 1.378(e) for reconsideration of decision on petition refusing to accept delayed payment of maintenance fee in an expired patent.
§ 1.741(b) – to accord a filing date to an application under §1.740 for extension of a patent term.

Petition Fees under 37 CFR 1.17(g): Fee $200 Fee code 1463
For petitions filed under:
§1.12 - for access to an assignment record.
§1.14 - for access to an application.
§1.47 - for filing by other than all the inventors or a person not the inventor.
§1.59 - for expungement of information.
§1.103(a) - to suspend action in an application.
§1.136(b) - for review of a request for extension of time when the provisions of section 1.136(a) are not available.
§1.295 - for review of refusal to publish a statutory invention registration.
§1.296 - to withdraw a request for publication of a statutory invention registration filed on or after the date the notice of intent to publish issued.
§1.377 – for review of decision refusing to accept and record payment of a maintenance fee filed prior to expiration of a patent.
§1.550(c) – for patent owner requests for extension of time in ex parte reexamination proceedings.
§1.956 – for patent owner requests for extension of time in inter partes reexamination proceedings.
§ 5.12 – for expedited handling of a foreign filing license.
§ 5.15 – for changing the scope of a license.
§ 5.25 – for retroactive license.

Petition Fees under 37 CFR 1.17(h): Fee $130 Fee Code 1464
For petitions filed under:
§1.19(g) – to request documents in a form other than that provided in this part.
§1.84 – for accepting color drawings or photographs.
§1.91 – for entry of a model or exhibit.
§1.102(d) – to make an application special.
§1.138(c) – to expressly abandon an application to avoid publication.
§1.313 – to withdraw an application from issue.
§1.314 – to defer issuance of a patent.

Name (Print/Type)	**Colin D. Barnitz**	*Registration No. (Attorney/Agent)*	35,061
Signature		*Date*	May 13, 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	10/767,074	Confirmation No. 6113
Applicant	:	Nobuyuki MINOWA	
Filed	:	January 30, 2004	
Title	:	DEVICE AND METHOD FOR PERFORMING INFORMATION PROCESSING USING PLURALITY OF PROCESSORS	
TC/AU	:	2186	
Examiner	:	TBD	
Docket No.	:	1309.43464X00	
Customer No.:		24956	

PETITION TO MAKE SPECIAL
UNDER 37 CFR §1.102(d) (MPEP §708.02(VIII))

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Applicants petition the Commissioner to make the above-identified application special in accordance with 37 CFR §1.102(d). In support of this Petition, pursuant to MPEP § 708.02(VIII), Applicants state the following.

(A) REQUIRED FEE

This Petition is accompanied by the fee set forth in 37 CFR § 1.117(h). A Credit Card Payment Form in the amount of $130 accompanies this Petition in satisfaction of the fee. The Commissioner is hereby authorized to charge any

additional payment due, or to credit any overpayment, to Deposit Account No. 50-1417.

(B) ALL CLAIMS ARE DIRECTED TO A SINGLE INVENTION

Claims 1-21 are pending in the application. All the pending claims of the application are directed to a single invention. If the Office determines that all claims in the application are not directed to a single invention, Applicant will make election without traverse as a prerequisite to the grant of special status.

The claimed invention, as set forth in independent claims 1, 13, and 20-23, is generally directed to information processing using a plurality of processors. Under amended independent claim 1, the invention is an information processing device which processes information using a plurality of processors, comprising: one or more first processors that have one or a plurality of first local memories; one or more second processors which directly write write information into a target first local memory that a target first processor selected from among said first processors has, and/or which directly read read information from said target first local memory; and an address map memory means for storing a first address map on which the first local memory addresses for each of said one or more first processors are recorded, wherein each of said one or more second processors acquires the first local memory address of said target first processor from said first address map, writes said write information into the acquired first local memory address, and/or reads said read information from the acquired first local memory address.

Additionally, under independent claim 13, the invention is a memory control device which comprises a plurality of microprocessors and a physical or logical memory device, and which performs memory control of the storage of information from host devices in said memory device using said plurality of microprocessors, comprising: one or more first microprocessors that have one or a plurality of first local memories; one or more second microprocessors; and a first address map memory part that stores a first address map on which the first local memory addresses for each of said one or more first microprocessors are recorded; wherein each of said one or more second microprocessors acquires, from said first address map, a first local memory write address indicating where writing is to be performed in a target first local memory which a target first microprocessor selected from among said first microprocessors has, and writes write information into the acquired first local memory write address.

Furthermore, under independent claim 20, the invention is a memory control device which comprises a plurality of microprocessors and a physical or logical memory device, and which controls the storage of information from host devices in said memory device using said plurality of microprocessors, this memory control device comprising: one or more first microprocessors that have one or a plurality of first local memories; one or more second microprocessors that have one or a plurality of second local memories; a first address map memory means for storing a first address map on which first local memory addresses for each of said one or more first microprocessors are recorded; and a second address map memory means

for storing a second address map on which second local memory addresses for each of said one or more second microprocessors are recorded; wherein a target second microprocessor selected from among said second microprocessors acquires, from the first address map, a first local memory write address indicating where writing is to be performed in a target first local memory which a target first microprocessor selected from among said first microprocessors has, and writes a read command into the acquired first local memory write address, and; wherein in response to the read command that is written into the first local memory write address, the target first microprocessor acquires, from the second address map, the second local memory write address of the target second microprocessor that originated said read command, reads out read information in the first local memory, and writes the read information into the acquired second local memory write address.

In addition, under independent claim 21, the invention is an information processing method which processes information using a plurality of processors, comprising the steps in which: each of one or more second microprocessors acquires a local memory address of a target first processor from an address map on which local memory addresses for each of one or more first processors having one or a plurality of local memories are recorded; and each of said one or more second processors writes write information into said acquired local memory address, and/or reads read information from said acquired local memory address.

Further, under independent claim 22, the invention is an information processing device which processes information using a plurality of processors,

comprising: one or more first processors that have one or a plurality of first local memories; one or more second processors which directly write write information into a target first local memory that a target first processor selected from among said first processors has, and/or which directly read read information from said target first local memory; and a relay device which receives said write information from said second processor side and transfers the write information to said first processor side, wherein said relay device comprises a relay memory, and when transferring said write information, said relay device selectively performs an operation of said transfer after said write information is temporarily stored in said relay memory, and an operation of said transfer without storing said write information in said relay memory.

Finally, under independent claim 23, the invention is an information processing method which processes information using a plurality of processors, comprising the steps in which: each of one or more second microprocessors acquires a local memory address of a target first processor from an address map on which local memory addresses for each of one or more first processors having one or a plurality of local memories are recorded; and each of said one or more second processors writes write information into said acquired local memory address, and/or reads read information from said acquired local memory address; and a relay device receives said write information from said second processor side and transfers the write information to said first processor side, wherein said relay device comprises a relay memory, and when transferring said write information, said relay device selectively performs an operation of said transfer after said write information is

temporarily stored in said relay memory, and an operation of said transfer without storing said write information in said relay memory.

(C) PRE-EXAMINATION SEARCH

A careful and thorough pre-examination search has been conducted, directed to the invention as claimed. The pre-examination search was conducted in the following US Manual of Classification areas:

Class	Subclass
370	229-231, 236, 389, 412, 414, 444
709	207, 213, 232-235, 250
710	6, 29, 52-57, 60
711	100, 111-114, 151, 154-158

Furthermore, a keyword search was conducted on the USPTO's EAST database, including the US patent database, the US published patent applications database, and the European and Japanese abstract databases.

(D) DOCUMENTS DEVELOPED BY THE PRE-EXAMINATION SEARCH AND OTHER ART OF RECORD IN THE APPLICATION

The documents located by the pre-examination search are listed below. These documents were made of record in the present application by the Information Disclosure Statement filed April 22, 2005.

Document No.	Inventor
US 5390299	Rege et al.
US 5710932	Hamanaka et al.
US 5740468	Hirose
US 5892979	Shiraki et al.
US 6212582	Chong et al.
US 6219728	Yin

Document No.	Inventor
US 6260120	Blumenau et al.
US 6275896	Kojima
US 6715007	Williams et al.
US 6851000	Lai
US 20030188085	Arakawa et al.

Additionally, a search was conducted regarding the British equivalent of the present application by an examiner in the British Patent Office, and an Examination Report was issued. The British Examination Report cited the following documents, which were made of record in the present application by the Information Disclosure Statement filed August 30, 2004.

Document No.	Inventor
EP 0326164	Hamanaka et al.
EP 0908825	Casamatta

Additionally, the following documents were made of record in the present application by the Information Disclosure Statement filed January 30, 2004.

Document No.	Inventor
US 5909540	Carter et al.
US 5918229	Davis et al.
US 5987506	Carter et al.
US 6026474	Carter et al.
US 6148377	Carter et al.
GB 2375621A	Thibault
JP 2001-306265A	Minowa et al.

Because all of the above-listed documents are already of record in the present application, in accordance with MPEP § 708.02(VIII)(D), additional copies of these documents have not been submitted with this Petition.

(E) DETAILED DISCUSSION OF THE REFERENCES

Those of the above-listed documents deemed to be most closely-related to the present matter encompassed by the claims are discussed below in section 2, pointing out, with the particularity required by 37 CFR 1.111 (b) and (c), how the claimed present matter is patentable over the teachings of these documents.

1. Discussion of the Invention

Under the invention, a memory control device controls access from host devices to a memory device. The memory control device may contain two or more channel adapters for communicating with host devices and two or more disk adapters for communicating with disk devices. One or more microprocessors (MPs) are installed in each of these channel adapters and disk adapters, and control information is exchanged between the MPs in the channel adapters and the MPs in the disk adapters. In the prior art the exchange of information was accomplished using polling of a shared memory. However, under the present invention, each MP may have a local memory, and an address map may be referred to by an MP for writing information to or reading information from a local memory of another MP. This reduces the time and burden on the MPs for acquiring the control information. (See, e.g., specification of the present application at pages 1-7 and 20-21.)

Accordingly, it is submitted that the present invention is patentable over the cited references because, as set forth in independent claim 1, the invention includes an information processing device having one or more first processors having local

memories, and one or more second processors that acquire from an address map a first local memory address of a target first processor, and writes write information into the acquired first local memory address, and/or reads read information from the acquired first local memory address. Independent method claims 21 and 23 are directed to similar subject matter in a method format.

Similarly, independent claims 13 and 20 of the present application provide for a memory control device with one or more first microprocessors that have first local memories, and one or more second microprocessors that acquire from an address map a first local memory write address of a target first local memory of a target first microprocessor, and writes information or a command into the acquired first local memory write address.

Additionally, independent claims 22 and 23 provide for an information processing device and method that includes a relay device which receives write information from the one or more second processors and transfers the write information to the target first processor, wherein the relay device includes a relay memory, and when transferring the write information, the relay device selectively performs an operation of the transfer after the write information is temporarily stored in the relay memory, or an operation of the transfer without storing the write information in the relay memory.

As will be discussed in more detail below, the prior art does not teach or suggest the above-described features.

2. Discussion of the References Deemed to be Most-Closely Related

The patent to Rege et al., US 5390299, discloses a communication interface adapter employing buffer memory in the transfer of data packets between a data network and a host computer. The system includes a network adapter including a packet buffer memory coupled to the network to store data packets received from the network, means for transferring the data packets from the packet buffer memory to the host computer and means for notifying the host computer when the occupancy of the packet buffer memory exceeds a threshold value. The means for notifying includes a means for setting an average threshold exceeded bit in a data word associated with one of the data packets to be delivered to the host computer, the average threshold being a predetermined average fullness level of the packet buffer memory, and a means for setting an instantaneous threshold exceeded bit in a data word associated with one of the data packets to be delivered to the host computer, the instantaneous threshold being a predetermined instantaneous fullness level of the packet buffer memory. When the buffer memory has insufficient free space to store an incoming packet, the packet is discarded. The network adapter keeps a count of the number of discarded packets. (See, e.g., Abstract and column 1, line 62, through column 2, line 28.) However, unlike the present invention, Rege et al. do not disclose the use of an address map for acquiring an address of a target local memory or a selective relay device for transferring the write information. Thus, Rege et al. do not disclose an information processing device or method in which one or more first processors have local memories, and one or more second processors

acquire from an address map a local memory address of a target first processor, and writes write information into the acquired first local memory address, and/or reads read information from the acquired first local memory address, as recited in claims 1, 21 and 23. Additionally, Rege et al. do not teach a memory control device with one or more first microprocessors that have first local memories, and one or more second microprocessors that acquire from an address map a first local memory write address of a target first local memory of a target first microprocessor, and writes information or a command into the acquired first local memory write address, as set forth in claims 13 and 20. Further, Rege et al. do not teach that a relay device receives the write information from the second processors and selectively performs an operation of transferring the write information either after temporarily storing the write information in the relay memory, or without storing the write information in the relay memory, as recited in claims 22 and 23.

The patent to Hamanaka et al., US 5710932 (equivalent to EP 0326164 to Hamanaka et al.) teaches a parallel computer having a plurality of processor elements, with a local memory being provided for each of the processor elements. Data to be sent to another processor is transferred with respect to an address of a local memory in a destination processor which is produced from a main group belonging to the data and also a sub-identifier for identifying the data to be sent from other data in the data group. (See, e.g., column 3, line 65, through column 5, line 42, and column 15, lines 7-43.) Thus, Hamanaka et al. do not provide an address

map for acquiring an address of a target local memory, or a selective relay device for transferring the write information. Accordingly, Hamanaka et al. do not disclose an information processing device or method in which one or more first processors have local memories, and one or more second processors acquire from an address map a local memory address of a target first processor, and writes write information into the acquired first local memory address, and/or reads read information from the acquired first local memory address, as recited in claims 1, 21 and 23. Neither do Hamanaka et al. teach a memory control device with one or more first microprocessors that have first local memories, and one or more second microprocessors that acquire from an address map a first local memory write address of a target first local memory of a target first microprocessor, and writes information or a command into the acquired first local memory write address, as set forth in claims 13 and 20. Further, Hamanaka et al. do not teach that a relay device receives the write information from the second processors and selectively performs an operation of transferring the write information either after temporarily storing the write information in the relay memory, or without storing the write information in the relay memory, as recited in claims 22 and 23.

The patent to Hirose, US 5740468, discloses data transferring buffer circuits for data exchange enabling data transfer between a great number of processors using data transferring buffer circuits for data exchange suitable for data transfer between processors by a relatively small number of buffers with relatively simple

control processors. The buffer circuits include: a plurality of buffers, corresponding to the plurality of data sources, independently receiving and storing data sent from the plurality of data sources; a buffer limit signal generating circuit for delivering a buffer limit signal when the amount of data stored in the buffer reaches a predetermined limit; a data read signal generating circuit for selecting one of the buffers and generating a data reading signal for the selected buffer based on the remaining data amount and information concerning the vacancy of the buffer to which data is to be supplied; and a selected data delivery circuit for adopting data selected by the data read signal generating circuit and delivering the adopted data. (See, e.g., Abstract and column 1, line 43 through column 2, line 25, and column 7, lines 22-33.) However, unlike the present invention, Hirose does not teach the use of an address map, or the use of a selective relay device. Thus, Hirose does not disclose an information processing device or method in which one or more first processors have local memories, and one or more second processors acquire from an address map a local memory address of a target first processor, and writes write information into the acquired first local memory address, and/or reads read information from the acquired first local memory address, as recited in claims 1, 21 and 23. Further Hirose does not show or suggest a memory control device with one or more first microprocessors that have first local memories, and one or more second microprocessors that acquire from an address map a first local memory write address of a target first local memory of a target first microprocessor, and writes information or a command into the acquired first local memory write address, as set

forth in claims 13 and 20. Nor does Hirose teach that a relay device receives the write information from the second processors and selectively performs an operation of transferring the write information either after temporarily storing the write information in the relay memory, or without storing the write information in the relay memory, as recited in claims 22 and 23.

The patent to Shiraki et al., US 5892979, discloses an overflow control unit that stores, in a FIFO buffer, data generated by a processor. The overflow control unit sets a predetermined flag, upon detecting that a FIFO buffer is full or nearly full. The overflow control unit stores, in a saving buffer, data sent from the processor, while the flag is set. Thereafter, the overflow control unit notifies the processor, by an interrupt, of an effect that an available capacity of the FIFO buffer rises above a predetermined threshold. Upon receiving an interrupt, the processor transfers to the FIFO buffer data saved in the saving buffer. Upon a completion of transferring to the FIFO buffer all data saved in the saving buffer, the processor resets the flag. This allows the overflow control unit to again store in the FIFO buffer, data sent from the processor. The overflow control unit also monitors the volume of data stored in the saving buffer, and notifies the processor, by an interrupt, of an effect that the saving buffer is full. Upon receiving an interrupt, the processor expands an available capacity of the saving buffer. (See, e.g., Abstract and column 2, line 12-39.) However, unlike the present invention, Shiraki et al. do not disclose the use of an address map by the processors, or the use of a selective relay device during transfer

of write data. Thus, Shiraki et al. do not disclose an information processing device or method in which one or more first processors have local memories, and one or more second processors acquire from an address map a local memory address of a target first processor, and writes write information into the acquired first local memory address, and/or reads read information from the acquired first local memory address, as recited in claims 1, 21 and 23. Nor does Shiraki et al. teach a memory control device with one or more first microprocessors that have first local memories, and one or more second microprocessors that acquire from an address map a first local memory write address of a target first local memory of a target first microprocessor, and writes information or a command into the acquired first local memory write address, as set forth in claims 13 and 20. Further, Shiraki et al. do not teach that a relay device receives the write information from the second processors and selectively performs an operation of transferring the write information either after temporarily storing the write information in the relay memory, or without storing the write information in the relay memory, as recited in claims 22 and 23.

The patent to Chong et al., US 6212582, discloses a method for controlling data packet traffic flow over a bus interconnecting two or more nodes in a data communication system, each node having a unique address with it and having a respective buffer memory for temporarily holding incoming data communicated, each node further being capable of multicast sending of data packets over the bus to one or more nodes having respective addresses logically associated with a unique

address. The method comprises checking current available buffer memory occupancy upon receipt of a data packet, the node being capable of outputting for transmission on the bus a first flow control indicator message when the data temporarily stored in the buffer memory is above a first buffer occupancy threshold associated with data of a first priority type, and a second flow control indicator message when the data temporarily stored in the buffer memory is above a second buffer occupancy threshold, the second buffer occupancy threshold being greater than the first occupancy threshold. The system implements a logical flow control to prevent the transmission of data packet traffic of the first priority from one or more sending nodes to two or more received nodes logically associated with the outputting node at the priority in response to receipt of the first flow control indicator message, and implements physical logical flow control to prevent transmission of data packet at any traffic priority in response to the second flow control indicator message. (See, e.g., Abstract and column 2, line 65, through column 3, line 29.) Thus, Chong et al. are concerned with a network, rather than an information processing device or a memory control device, as in the present invention. Additionally, Chong et al. use multicast sending, rather than sending to a targeted processor. Further, Chong does not mention reading information from a processor local memory or the use of a selective relay device. Accordingly Chong et al. do not disclose an information processing device or method in which one or more first processors have local memories, and one or more second processors acquire from an address map a local memory address of a target first processor, and writes write information into the

acquired first local memory address, and/or reads read information from the acquired first local memory address, as recited in claims 1, 21 and 23. Further, Chong et al. do not teach a memory control device with one or more first microprocessors that have first local memories, and one or more second microprocessors that acquire from an address map a first local memory write address of a target first local memory of a target first microprocessor, and writes information or a command into the acquired first local memory write address, as set forth in claims 13 and 20. Nor do Chong et al. teach that a relay device receives the write information from the second processors and selectively performs an operation of transferring the write information either after temporarily storing the write information in the relay memory, or without storing the write information in the relay memory, as recited in claims 22 and 23.

The patent to Yin, US 6219728, discloses a method and apparatus for allocating shared memory resources and discarding incoming data as necessary. Adaptive thresholds are provided for each individual queue or port. The adaptive thresholds are adjusted in response to changes in the overall usage of the shared memory resources. As memory usage increases, each threshold value is lowered. When memory usage decreases, each threshold value is increased. The apparatus also includes a system for allocating shared memory resources among a plurality of queues. The shared memory resources are monitored to determine a number of available memory buffers in the shared memory. Threshold values are generated for each queue indicating the number of data cells to be stored in the associated queue.

The threshold values are updated in response to changes in the number of available memory buffers. The apparatus also performs a comparison of the threshold value with the queue usage to determine whether to accept or discard incoming data cells destined for the queue. The apparatus adjusts the threshold values by increasing the threshold value in response to increased available memory and decreasing the threshold value in response to decreased available memory. (See, e.g., Abstract and column 2, lines 27-54.) However, unlike the present invention, Yin uses a shared memory, rather than local memories. Further, Yin does not teach an address map for local memories, or the use of a selective relay device. Thus, Yin does not disclose an information processing device or method in which one or more first processors have local memories, and one or more second processors acquire from an address map a local memory address of a target first processor, and writes write information into the acquired first local memory address, and/or reads read information from the acquired first local memory address, as recited in claims 1, 21 and 23. Also, Yin does not teach a memory control device with one or more first microprocessors that have first local memories, and one or more second microprocessors that acquire from an address map a first local memory write address of a target first local memory of a target first microprocessor, and writes information or a command into the acquired first local memory write address, as set forth in claims 13 and 20. Further, Yin does not teach that a relay device receives the write information from the second processors and selectively performs an operation of transferring the write information either after temporarily storing the write

information in the relay memory, or without storing the write information in the relay memory, as recited in claims 22 and 23.

The patent to Blumenau et al., US 6260120, discloses a storage controller for controlling access to data storage has a memory and at least one data port for a data network including host processors. The memory is programmed to define a respective specification for each host processor of a respective subset of the data storage to which access by the host processor is restricted, and each specification is associated with a host identifier stored in the memory. When the storage controller receives a data access request from a host processor, it decodes a host identifier from the data access request, and searches the memory for a host identifier matching the host identifier decoded from the request. Upon finding a match, the respective specification of the respective subset for the host processor is accessed to determine whether or not storage specified by the storage access request is contained in the respective subset. If so, then storage access can continue, and otherwise, storage access is denied. Preferably the host identifier decoded from the request is a temporary address assigned by the network, and also stored in the memory in association with each respective specification is a relatively permanent identifier for the host processor. The storage controller includes a cache memory and a plurality of port adapters each having at least one data port for connecting the storage controller to a plurality of the host processors, and each of the port adapters has a respective memory for storing temporary identifiers of hosts having logged in

to the port adapters in association with a specification of a respective subset of the data storage to which access through each of the port adapters by each of the hosts is restricted, and wherein the cache memory stores the relatively permanent identifiers of the hosts having logged into the port adapters. (See, e.g., Abstract and column 2, line 44, through column 3, line 18.) However, unlike the present invention, Blumenau et al. do not disclose the use of an address map for local memories, or the use of a selective relay device. Thus, Blumenau et al. do not disclose an information processing device or method in which one or more first processors have local memories, and one or more second processors acquire from an address map a local memory address of a target first processor, and writes write information into the acquired first local memory address, and/or reads read information from the acquired first local memory address, as recited in claims 1, 21 and 23. Further, Blumenau et al. do not teach a memory control device with one or more first microprocessors that have first local memories, and one or more second microprocessors that acquire from an address map a first local memory write address of a target first local memory of a target first microprocessor, and writes information or a command into the acquired first local memory write address, as set forth in claims 13 and 20. Nor do Blumenau et al. teach that a relay device receives the write information from the second processors and selectively performs an operation of transferring the write information either after temporarily storing the write information in the relay memory, or without storing the write information in the relay memory, as recited in claims 22 and 23.

The patent to Kojima, US 6275896, discloses a data transfer method and apparatus for performing fast data transfer between a first storage medium and a second storage medium and a data input/output controlling method and apparatus. The data transfer apparatus comprises a temporary storing means for temporarily storing data reproduced from the first storage medium and data reproduced from the second storage medium. A storage state monitoring means monitors the state of storage of the temporary storing means; and a transfer rate controlling means controls the transfer rate of the data reproduced from the first storage medium and the data reproduced from the second storage medium based on a signal indicating the state of the storage input from the storage state monitoring means. A system controller continuously monitors whether the amount of data which can be stored in the temporary storage is over a predetermined threshold. When the system controller decides that the amount of data which can be stored in the temporary storage is over the predetermined threshold, system controller decreases the transfer rate. (See, e.g., Abstract and column 2, lines 12-18, column 4, lines 16-56, and column 6, lines 12-18.) However, unlike the present invention, Kojima does not disclose the use of an address map for local memories, or the use of a selective relay device. Thus, Kojima does not disclose an information processing device or method in which one or more first processors have local memories, and one or more second processors acquire from an address map a local memory address of a target first processor, and writes write information into the acquired first local memory

address, and/or reads read information from the acquired first local memory address, as recited in claims 1, 21 and 23. Further, Kojima does not show or suggest a memory control device with one or more first microprocessors that have first local memories, and one or more second microprocessors that acquire from an address map a first local memory write address of a target first local memory of a target first microprocessor, and writes information or a command into the acquired first local memory write address, as set forth in claims 13 and 20. Nor does Kojima teach that a relay device receives the write information from the second processors and selectively performs an operation of transferring the write information either after temporarily storing the write information in the relay memory, or without storing the write information in the relay memory, as recited in claims 22 and 23.

The patent to Williams et al., US 6715007, discloses a communication system in which flow of data that is regulated. A data rate is established in each of the data sources and data receivers. The data is transmitted by the data source and written into a buffer at the source data rate, and then the data is read from the buffer and transmitted to the data receiver at the receiver data rate. The level of data in the buffer is monitored, and a rate control signal is dispatched to either the data source or the receiver when it is determined that the buffer data level is increasing or decreasing while at a lower or upper data level threshold. Subsequently, either the source or receiver data rate is adjusted in response to the rate control signal. (See, e.g., Abstract and column 2, lines 8-30.) However, unlike the present invention,

Williams et al. do not disclose an address map for local memories, or a selective relay device. Thus, Williams et al. do not disclose an information processing device or method in which one or more first processors have local memories, and one or more second processors acquire from an address map a local memory address of a target first processor, and writes write information into the acquired first local memory address, and/or reads read information from the acquired first local memory address, as recited in claims 1, 21 and 23. Neither do Williams et al. teach a memory control device with one or more first microprocessors that have first local memories, and one or more second microprocessors that acquire from an address map a first local memory write address of a target first local memory of a target first microprocessor, and writes information or a command into the acquired first local memory write address, as set forth in claims 13 and 20. Further, Williams et al. do not teach that a relay device receives the write information from the second processors and selectively performs an operation of transferring the write information either after temporarily storing the write information in the relay memory, or without storing the write information in the relay memory, as recited in claims 22 and 23.

The patent to Lai, US 6851000, discloses method and apparatus of flow control management of data packets in a switch. The method has steps of: determining each time data is being written to memory in order to calculate a memory used amount; determining each time data is being freed from the memory in order to calculate a memory freed amount; and calculating how much total memory

is being used using the memory freed amount and the memory used amount. A comparison is made by comparing the total memory being used to a first predetermined threshold. When the first predetermined threshold is reached, a first predetermined threshold command is issued indicating that the first predetermined threshold has been reached. (See, e.g., Abstract and column 2, line 19, through column 3, line 27.) However, unlike the present invention, Lai does not disclose an address map for local memories, or a selective relay device. Thus, Lai does not disclose an information processing device or method in which one or more first processors have local memories, and one or more second processors acquire from an address map a local memory address of a target first processor, and writes write information into the acquired first local memory address, and/or reads read information from the acquired first local memory address, as recited in claims 1, 21 and 23. Further, Lai does not teach a memory control device with one or more first microprocessors that have first local memories, and one or more second microprocessors that acquire from an address map a first local memory write address of a target first local memory of a target first microprocessor, and writes information or a command into the acquired first local memory write address, as set forth in claims 13 and 20. Nor does Lai teach that a relay device receives the write information from the second processors and selectively performs an operation of transferring the write information either after temporarily storing the write information in the relay memory, or without storing the write information in the relay memory, as recited in claims 22 and 23.

The published patent application to Arakawa et al., US 20030188085, discloses a storage system and a control method for the storage system, in which a plurality of storage system nodes is made operable as a single storage system. The clustered storage system is operable as a single storage system, and includes a process to allow the system administrator or the user to correlate data, particularly logical volume, stored and used in the clustered storage system with a node that processes the data and to manage such data. The clustered storage system in which a plurality of storage systems operates as a single storage system includes: a process that obtains the configuration of resources, as well as at least one of resource size used and resource usage load, of the storage system used in processing data that the storage system has and that is stored in the storage system; a process that presents the relations between address information which is provided by the clustered storage system and resource information of each storage system to a computer that uses the data, and a process that presents resource information based on such relations. (See, e.g., Abstract and paragraphs 15-20.) However, unlike the present invention, Arakawa et al. do not disclose an address map for local memories, or a selective relay device. Thus, Arakawa et al. do not disclose an information processing device or method in which one or more first processors have local memories, and one or more second processors acquire from an address map a local memory address of a target first processor, and writes write information into the acquired first local memory address, and/or reads read

information from the acquired first local memory address, as recited in claims 1, 21 and 23. Similarly, Arakawa et al. do not teach a memory control device with one or more first microprocessors that have first local memories, and one or more second microprocessors that acquire from an address map a first local memory write address of a target first local memory of a target first microprocessor, and writes information or a command into the acquired first local memory write address, as set forth in claims 13 and 20. Further, Arakawa et al. do not teach that a relay device receives the write information from the second processors and selectively performs an operation of transferring the write information either after temporarily storing the write information in the relay memory, or without storing the write information in the relay memory, as recited in claims 22 and 23.

The European Patent Application to Hamanaka et al., EP 0326164, is equivalent to US Patent No. 5710932, to Hamanaka et al., discussed above. Accordingly, this reference is distinguished for the same reasons recited above with respect to the US equivalent.

The European Patent Application to Casamatta, EP 0908825, shows a data processing system having a plurality of nodes wherein each node has at least one processor and a local memory. Each memory module location is accessed by only one memory address. A translation table can be written upon booting and addressed by suitable address fields, and output module-selection signals or codes.

(See, e.g. paragraphs 45-51 and 80-96.) However, Casamatta does not teach a processor that writes data to a targeted memory address of a targeted processor, or a selective relay device. Accordingly, Casamatta does not disclose an information processing device or method in which one or more first processors have local memories, and one or more second processors acquire from an address map a local memory address of a target first processor, and writes write information into the acquired first local memory address, and/or reads read information from the acquired first local memory address, as recited in claims 1, 21 and 23. Neither does Casamatta teach a memory control device with one or more first microprocessors that have first local memories, and one or more second microprocessors that acquire from an address map a first local memory write address of a target first local memory of a target first microprocessor, and writes information or a command into the acquired first local memory write address, as set forth in claims 13 and 20. Further, Casamatta does not teach that a relay device receives the write information from the second processors and selectively performs an operation of transferring the write information either after temporarily storing the write information in the relay memory, or without storing the write information in the relay memory, as recited in claims 22 and 23.

3. Remaining References

The remaining references of record in the application are deemed to not be most-closely related to the present invention, and/or were provided as background

information, and also do not show or suggest the present invention. For example, the patents to Carter et al. and Davis et al. (US 5909540, US 5918229, US 5987506, US 6026474, US 614837) all teach a shared memory, as does the British patent to Thibault, (GB 2375621A). The Japanese patent application to Minowa, JP 2001-306265A, is discussed as background in the specification of the present application at page 2, and also teaches a shared memory. Thus, none of these documents teach the use of an address map for local memories, or the use of a selective relay device for transferring write information.

CONCLUSION

From the above discussion, it is apparent that none of the art of record shows or suggests the present invention, including an information processing device or method in which one or more first processors have local memories, and one or more second processors acquire from an address map a local memory address of a target first processor, and writes write information into the acquired first local memory address, and/or reads read information from the acquired first local memory address, as recited in claims 1, 21 and 23. Nor does the art of record show or suggest a memory control device with one or more first microprocessors that have first local memories, and one or more second microprocessors that acquire from an address map a first local memory write address of a target first local memory of a target first microprocessor, and writes information or a command into the acquired first local memory write address, as recited in claims 13 and 20. Further, the art of record

does not teach that a relay device receives the write information from the second processors and selectively performs an operation of transferring the write information either after temporarily storing the write information in the relay memory, or without storing the write information in the relay memory, as recited in claims 22 and 23. Accordingly, claims 1, 13 and 20-23 are patentable over the cited references.

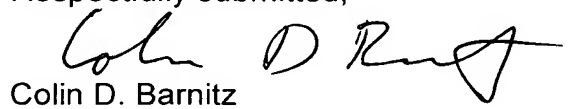
The Applicants submit that the foregoing discussion demonstrates the patentability of the independent claims over the closest-known prior art, taken either singly, or in combination. The remaining claims depend from the independent claims, claim additional features of the invention, and are patentable at least because they depend from allowable base claims. Accordingly, the requirements of 37 CFR §1.102(d) having been satisfied, the Applicants request that this Petition to Make Special be granted and that the application be examined according to prescribed procedures set forth in MPEP §708.02 (VIII).

The Applicants prepared this Petition in order to satisfy the requirements of 37 C.F.R. §1.102(d) and MPEP §708.02 (VIII). The pre-examination search required by these sections was "directed to the invention as claimed in the application for which special status is requested." MPEP §708.02 (VIII). The search performed in support of this Petition is believed to be in full compliance with the requirements of MPEP §708.02 (VIII); however, Applicants make no representation that the search covered every conceivable search area that might contain relevant prior art. It is always possible that prior art of greater relevance to the claims may exist. The Applicants urge the Examiner to conduct his or her own complete search of the prior art, and to

thoroughly examine this application in view of the prior art cited above and any other prior art that may be located by the Examiner's independent search.

Further, while the Applicants have identified and discussed certain portions of each cited reference in order to satisfy the requirement for a "detailed discussion of the references, which discussion points out, with the particularly required by 37 C.F.R. §1.111(b) and (c), how the claimed subject matter is patentable over the references" (MPEP §708.02(VIII)), the Examiner should not limit review of these documents to the identified portions, but rather is urged to review and consider the entirety of each reference.

Respectfully submitted,



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